GaAs IC DIRECT-COUPLED AMPLIFIERS

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ABSTRACT

Performance of six different direct-coupled GaAs IC amplifiers, with bandwidths up to 4.5 GHz, is described, along with that of one similar ac-coupled amplifier. Statistical data on gain, bandwidth, distortion, and noise is presented. The effectiveness of inductor peaking, resistive loads, and variable feedback is discussed.

Introduction

Previously reported GaAs MESFET monolithic integrated-circuit amplifiers have been narrow-band designs with passive tuning elements in C- and X-band.[1,2,3] A single exception is the report by Van Tuyl[4] of dc-coupled amplifiers with 4-GHz upper corner (-1 dB) frequencies. For this design approach, the absence of passive tuning restricts the frequency range to about 4 GHz with present geometries, but makes possible multi-octave applications and reduces circuit area by one to two orders of magnitude, with a similar effect on cost.

This paper presents experimental results on amplifiers which extend the direct-coupled design approach in several ways, including gain, bandwidth, and output power. All are capable of driving a 50-ohm load. (The voltage amplifiers of Ref. 4 use small monitor FET's at input and output, avoiding the bandwidth limitation associated with driving a large output FET for gain into 50 ohms.)

Amplifier Descriptions

Each amplifier consists of one or more of either the open-loop or the feedback stages of Figure 1, or variations to be described, driving a relatively large output FET. Table 1 summarizes the amplifier configurations.

All designs were based on computer simulations with either ASTAP[5] or OPNODE[6]; additional details are given elsewhere in this volume.[8]

Figure 2 shows typical measured gain and bandwidth for the seven amplifier types, which are further described in the following sections.

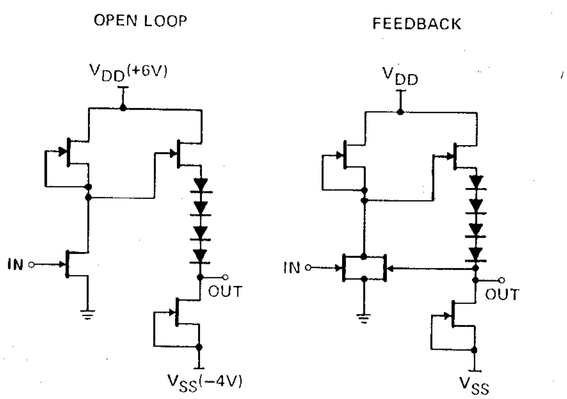

Fig. 1 Direct-Coupled GaAs IC Amplifier Stages.

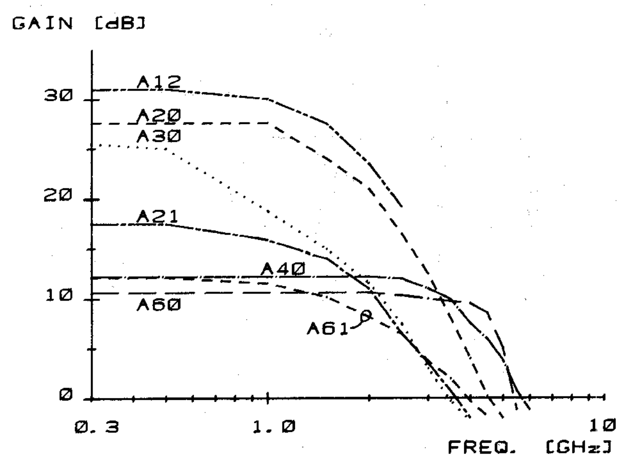

Fig. 2 Frequency Response of GaAs IC Amplifiers; R_L=50 ohms, V_{DD}=+6V, V_{SS}=-4V.

TABLE 1

CIRCUIT TYPE	STAGE 1	STAGE 2	STAGE 3	OUTPUT FET WIDTH (μ)	NOTES
A12	OL-30*	OL-30	FB-40	200	AC-Coupled
A20	OL-40	FB-40	FB-80	400	
A21	FB-60	FB-120	-----	1000	
A30	OL-60	OL-120	-----	400	Variable Feedback Around Stage 2
A40	FB-60	FB-120	-----	400	
A60	FB-120	-----	-----	500	Inductor Peaking
A61	OL-120	-----	-----	500	Bulk-Resistor Load, Inductor Peaking

* "OL" indicates open-loop stage (see Figure 1); "FB" inducates feedback stage. Number indicates device width in microns (width of inverter FET for open-loop stage, width of inverter FET plus feedback FET for feedback stage). Source-follower and current-source FET's are same width, active-load FET is half this width.

Amplifier Performance

Wide-Bandwidth Amplifiers

The highest bandwidth, 4.5 GHz, was obtained with the aid of a single peaking inductor between the inverter and source-follower portions of a feedback-amplifier stage (A60-Fig. 3 (a)). Theoretical and experimental data were used to design the 13 nH square-spiral inductor, which takes up as much space as all the active circuitry on the chip, despite utilizing 3-micron lines and spaces. A chip photograph is shown in Figure 4 (a). This circuit achieved better bandwidth at lower power dissipation than the best totally active design (A40-Figures 3 (b) and 4 (b)).

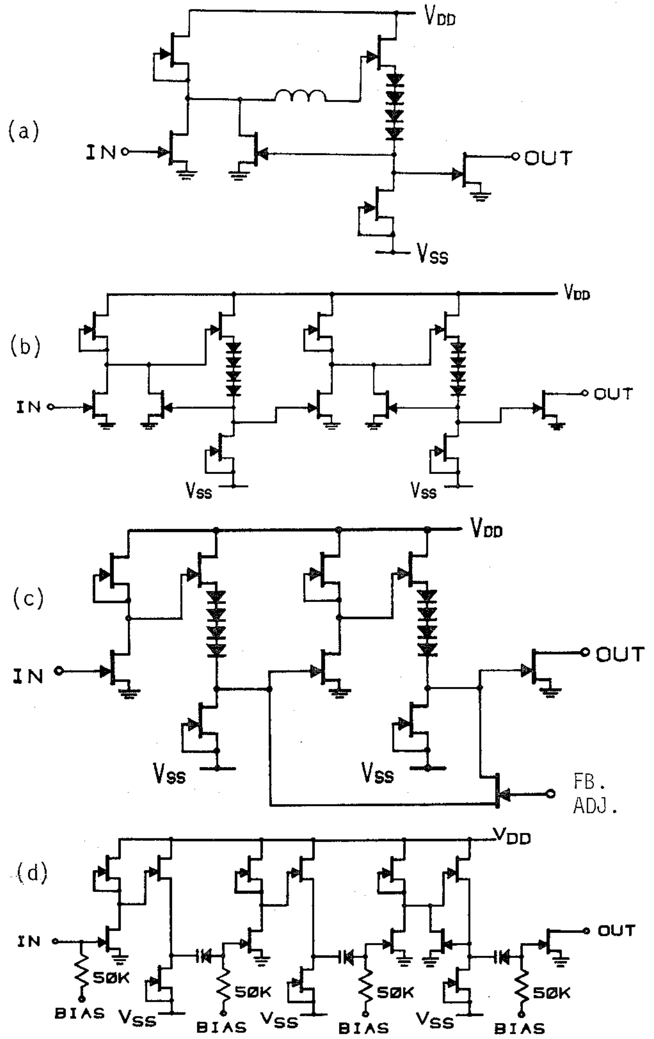

Fig. 3 Circuit Schematics For (a) A60, (b) A40 and A21, (c) A30, and (d) A12 Amplifiers.

Low-Distortion Amplifiers

Low-distortion applications were addressed with three different approaches: a) a large output FET, b) feedback, and c) a resistor in place of the active load. The large-output-FET amplifier, designated A21, was identical schematically to Figure 3 (b), but used a 1000-micron output FET in place of a 400-micron FET. It provided 10 dBm output power into 50 ohms with low harmonic distortion (Figure 5 (a)). A second low-distortion design (A30) used variable feedback around a full stage, the stage which contributes the most to distortion (Figure 3 (c)). The third low-distortion design (A61) made use of a bulk GaAs 300 ohm resistor in place of the less linear active-load device of the A60 version, with the same peaking inductor. Both of the latter approaches were less successful than the 1000-micron output design for minimizing distortion (Figure 5 (a) and (b)). Other amplifiers achieved harmonic performance similar to the 1000-micron-output version only at 5 dBm output power (Figure 5 (b)), except for the inductor-peaked (A60) design. Energy storage in the inductor helped to overcome the slew-rate effect limiting high-frequency output power, so that this circuit performed better than the 1000-micron-output design at high frequencies (Figure 5 (a)).

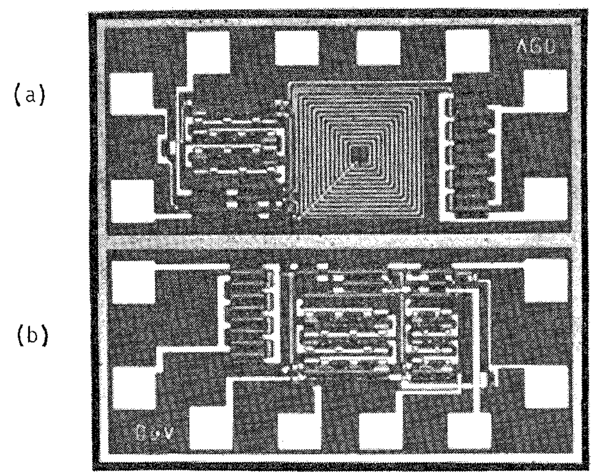

Fig. 4 Photograph of (a) A60 and (b) A40 Amplifiers; Chip Size is 300 x 650 Microns

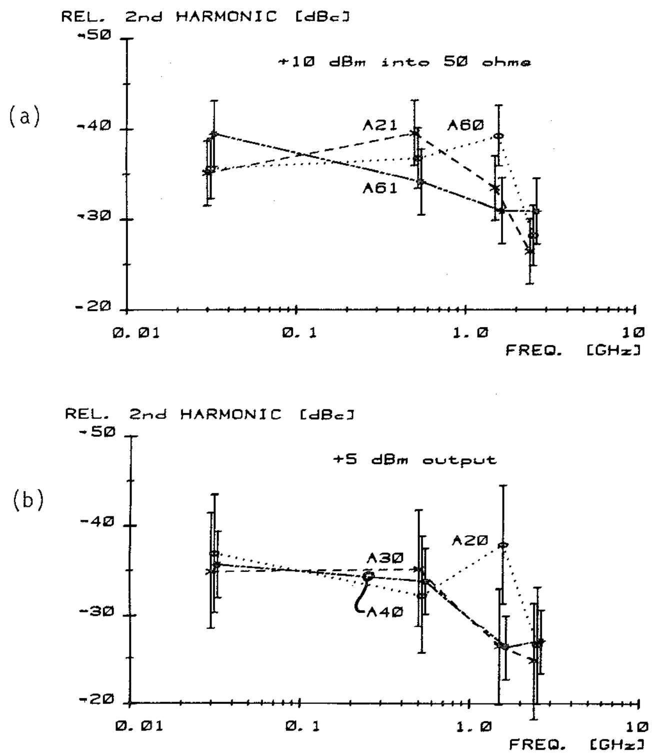

Fig. 5 Harmonic performance of various amplifiers at (a) +10 dBm and (b) +5 dBm output. Data is average for typically 20 chips; bars indicate one standard deviation above and below average.

AC-Coupled Amplifier

A low power-dissipation, ac-coupled design (A12-Fig. 3(d)) took advantage of varactor-diode coupling capacitors to eliminate the level-shift diodes and V_{SS} power supply; the three-stage amplifier had 30 dB gain and 2 MHz to 1.5 GHz bandwidth at the -3 dB points. Average dissipation was 420 mW, 30% lower than for any of the other designs. Dissipated power could be further reduced to about half this value by eliminating the buffer stages (source-follower and current-source MESFET's); however, bandwidth would be cut roughly in half as well.

Gain Variations

Chip-to-chip variations of gain were greatest for the amplifiers with the most stages, as expected. For example, the three-stage dc-coupled amplifier (A20) had a standard deviation of gain equal to 2.42 dB at 500 MHz (for 119 chips from 7 wafers), and 1.98 dB at 2.4 GHz -- which is one measure of bandwidth variation, since 2.4 GHz is above the amplifier's corner frequency. By comparison, the standard deviation for the 500 MHz gain of the single-stage inductor-peaked amplifier (A60) was 0.93 dB (for 81 chips from 5 of the above 7 wafers).

Noise Figure

Noise figure was close to computer simulations for white noise relative to a 50 ohm input termination; some representative values are: 16.8 dB average (0.84 dB standard deviation) for the dc-coupled three-stage design (A20) at 1.5 GHz, and 16.4 dB average (0.68 dB standard deviation) for the inductor-peaked active-load version (A60) at 1.5 GHz. This moderately high noise figure is due both to the contributions of the active-load and source-follower FET's, and to the lack of impedance matching to the amplifier's high optimum-noise input impedance. The 1/f-noise corner frequency was similar to that reported for discrete FET's (7), approximately 100 MHz, regardless of amplifier type.

Microwave Wafer Testing

Microwave characterization of over five hundred circuits, from a number of wafers, has formed the statistical base for the data presented above. The key elements of the test system which made this volume of testing possible were a thin-film probe card, which maintained 50-ohm lines to within 1 mm of the IC wafer; and a Hewlett Packard 8566A Spectrum Analyzer, which performed all gain, power, harmonic, and noise measurements under calculator control.

Conclusion

Production of the type of circuits described, along with companion linear circuits under investigation, should make possible compact, low-cost versions of systems which heretofore could only be realized in hybrid form.

Acknowledgement

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